



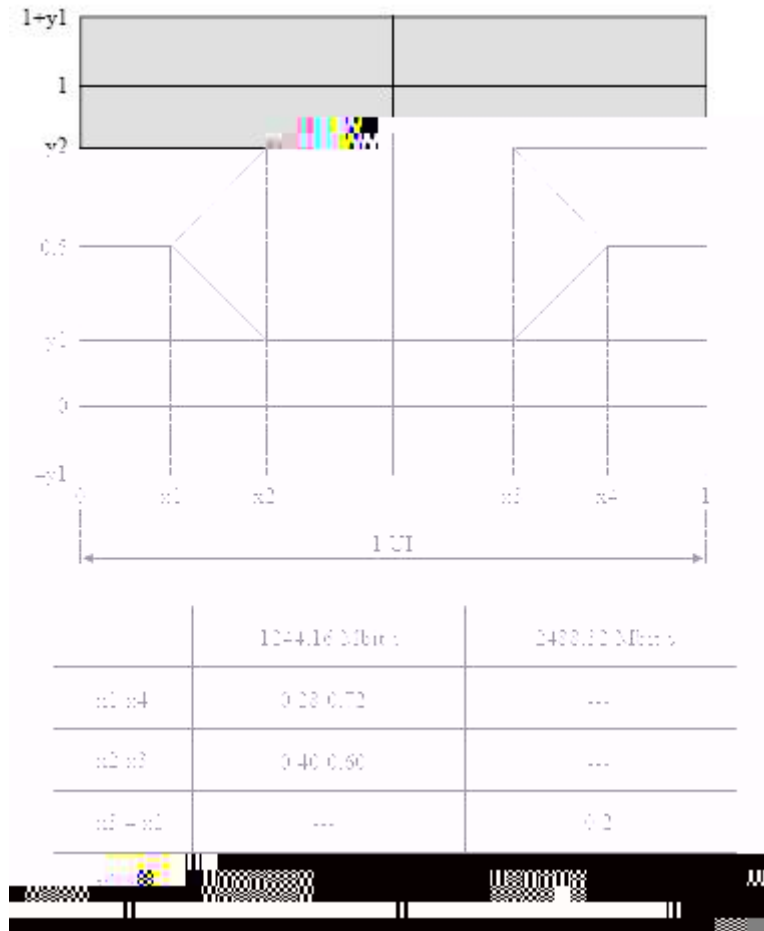
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**Note7:** Measured with PRBS 2<sup>23</sup>-1 test pattern @1.244Gbps with Tx on, ER=10dB, BER<=10E-10.

**Note8:** Time from the arrival of data to the output data settling to within 15% of final amplitude and duty-cycle. It is shown in the Figure 1.

**Note9:** Time from a falling edge on reset signal input to the start of preamble at the data input of the receiver.

**Note10:** DC coupled internal. Need LVPECL terminal on the hostboard.

**Note11:** Time from end of previous data burst to beginning of next data burst.

**Note12** Measured with PRBS23 Burst data pattern @1.244Gbps.